REMARKS

Reconsideration and allowance of the above reference application are respectfully requested.

Claims 1-15 and 17-22 stand rejected under 35 U.S.C. 102 as allegedly being anticipated by Favor et al. In response, claim 1 is canceled and is replaced by new claim 23. Claim 19 is canceled and is replaced by new claim 25. The remaining claims are amended to obviate the rejection.

Figure 5 shows the instructions being loaded into a "register" here multiplexer 525. For this reason, the drawing objection is respectfully traversed.

Specifically, Favor et al teaches a system where the instructions from main memory 130 are loaded into an instruction cache via a pre-decoder 270. The pre-decoder is capable of determining the width of a variable length instruction. See generally column 5 lines 20-49. However, the present system, as now claimed, includes significant distinctions over Favor et al.

Claim 23, for example, defines that each instruction source is "associated with a different location in an instruction pipeline". Favor et al teaches nothing about this subject matter; in fact, the interpretation of the present claims uses main memory 112, and L2 cache 122 as the instruction sources.

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This is certainly not associated with multiple locations in a pipeline, as claimed.

Claim 24 defines an additional aspect, that the receiving instructions receives multiple instructions simultaneously. Nothing in Favor et al teaches a plurality of instructions of varying sizes being decoded simultaneously. The pre-decoder 270 apparently only determines information about a single bit instruction at a time, see for example Favor et al column 5, line 50. Nowhere is there any teaching or suggestion that multiple different instruction bytes can be received at once, along with their size information and number information as claimed, and decoded in this way. Therefore, claim 24 should be additionally allowable.

Dependent claims 5 and 6 should be the allowable on their own merits, for reasons discussed above.

Claim 9 has been amended to include the limitation described above, that the information comes from different locations in an instruction pipeline. This is not taught or suggested by the cited prior art; see above.

Moreover, claim 9 defines loading the instructions simultaneously, and determining sizes of a plurality of instructions, which again is patentable over the cited prior art.

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Claim 14 has been amended in a similar way, and should be allowable, since it defines the information comes from different locations in an instruction pipeline, and also defines that the decoder receives the size and number of the plurality of instructions. Favor et al never teaches or suggests a number of decoding elements.

Claim 25 defines a switching element which switches both the instructions, and the instruction size information at the same time. Again, this is not taught or suggested by the cited prior art.

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

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Application Serial No. 09/675,815
Attorney's Docket No.: Intel 10559-274001 / P9281 - ADI APD1797-1-US

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Respectfully submitted,

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